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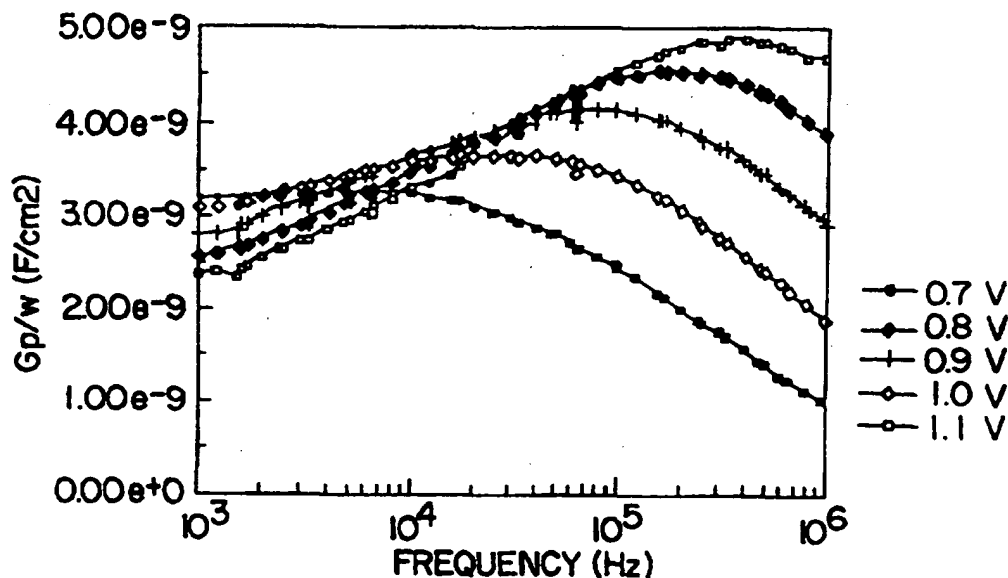
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(54) Title: PROCESS FOR REDUCING DEFECTS IN OXIDE LAYERS ON SILICON CARBIDE



## (57) Abstract

A method is disclosed for obtaining improved oxide layers and resulting improved performance from oxide based devices. The method comprises exposing an oxide layer on a silicon carbide layer to an oxidizing source gas at a temperature below the temperature at which SiC would begin to oxidize at a significant rate, while high enough to enable the oxidizing source gas to diffuse into the oxide layer, and while avoiding any substantial additional oxidation of the silicon carbide, and for a time sufficient to densify the oxide layer and improve the interface between the oxide layer and the silicon carbide layer.

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## PROCESS FOR REDUCING DEFECTS IN OXIDE LAYERS ON SILICON CARBIDE

### Field of the Invention

The present invention relates to an improved method for forming oxides on silicon carbide semiconductor material, and in particular relates to  
5 improving the oxides and the oxide interfaces in silicon carbide based metal oxide semiconductor (MOS) devices.

### Background of the Invention

Silicon carbide (SiC) has a combination of  
10 electrical and physical properties that make it attractive for a semiconductor material for high temperature, high voltage, high frequency and high power electronic devices. These properties include a  
3.0 electron-volt (eV) bandgap, a 4 millivolt per  
15 centimeter (MV/cm) electric field breakdown, a 4.9 W/cm<sup>2</sup>K thermal conductivity, and a 2.0x10<sup>7</sup> centimeter per second (cm/s) electron drift velocity.  
Furthermore, because SiC will grow thermal oxides, it offers significant advantages over other compound  
20 semiconductors. In particular, the ability to form a thermal oxide raises the corresponding ability to form metal-oxide-semiconductor (MOS) devices, including MOS field-effect transistors (MOSFETS) insulated gate  
bipolar transistors (IGBT's), MOS-controlled thyristors  
25 (MCTs), and other related devices. In turn, MOSFETs are extremely important devices in large scale integrated circuits. Accordingly, taking full advantage of SiC's electronic properties in MOS devices and resulting integrated circuits requires appropriate  
30 SiC oxidation technology.

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In spite of these advantageous characteristics, the quality of oxides on silicon carbide (SiC) has been a major obstacle to developing silicon carbide MOS devices. Oxide charge and interface states in particular, have an adverse effect on MOS device performance. Indeed, with the exception of substrate crystal growth, oxide quality is perhaps the largest barrier to advanced SiC MOS power devices and MOS integrated circuits. Oxides on SiC have been widely reported to have unacceptably high interface state densities and fixed oxide charge for MOS applications.

As used herein, the term "state" refers to a characteristic of a material, such as an available energy level position, and often defined using quantum mechanics. The existence of "states" in materials is not necessarily good or bad, and their presence or absence is probably better defined as desired or undesired. In the case of oxide layers on silicon carbide, the states appear to produce undesired operating characteristics in resulting devices, and thus are desirably minimized whenever possible.

Previous work comparing thermal oxidation techniques and investigating SiC/SiO<sub>2</sub> defects have led to only a few general observations: (1) wet oxides (i.e. those thermally grown in the presence of water vapor) have lower oxide charge and interface state densities than dry oxides (S. M. Tang, W. B. Berry, R. Kwor, M. V. Zeller and L. G. Matus, J. Electrochem. Soc., 137(1) p.221 (1990); S. Zaima, K. Onoda, Y. Koide, and Y. Yasuda, J. Appl. Phys., 68(12) p. 6304 (1990)); (2) the Si-face of SiC wafers oxidizes more slowly, but has lower oxide charge densities, than the carbon (C) face (Nitya N. Singh and Andrew Rys, Inst. Phys. Conf. Ser. No 137: Chapter 3, p. 325 (1993)); (3) oxides grown on n-type wafers have fewer interface states (Dale M. Brown, Mario Ghezzi, James Kretchmer,

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Evan Downey, Joseph Pimbley, and John Palmour, *IEEE Trans on Electron Devices*, Vol. 41, No. 4, p. 618 (1994)); T. Ouisse, N. Becourt, F. Templier, C. Jaussaud, *J. Appl. Phys.* 75(1) (1994); Singh, *supra*)  
 5 and lower oxide charge densities (Brown, *supra*; M. Shinohara, M. Yamanoka, S. Misawa, H. Okumura, S. Yoshida, *Jap.J.Appl.Phys.* 30(2) p.240 (1991); Singh, *supra*) than those grown on p-type wafers; and (4) contrary to early projections (Brown, *supra*), there is  
 10 no difference between boron (B) and aluminum (Al) as a p-type dopant in SiC (J.N. Shenoy, L.A. Lipkin, G.L. Chindalore, J. Pan, J.A. Cooper, Jr., J.W.Palmour, and M.R. Melloch, *Inst. Phys. Conf. Ser. No 141: Chapter 4*, p. 449 (1994)).

15 It will be understood that for the most part, the accuracy of these measurements and the resulting conclusions can vary to a greater or lesser extent, and should be evaluated and understood in that light.

Although these particular conclusions are  
 20 widely accepted, the quantification of the net oxide charge ( $Q_{ox}$ ) and interface state densities ( $D_{it}$ ) has varied widely, even when measuring the same crystal orientation, oxide thickness, dopant type and dopant species. These variations are demonstrated in Table 1,  
 25 which summarizes the oxide charge and interface state densities of SiO<sub>2</sub> on SiC as reported by various authors. The reported oxide thicknesses range from 500-600Å, except for the 200Å oxides on n-type samples of reference reported by Weiss, *supra*.

30

TABLE 1

Substrate/ Oxide	$Q_{ox}$ (cm <sup>-2</sup> )	$D_{it}$ (cm <sup>-2</sup> eV <sup>-1</sup> )
N-6H/dry	0-1x10 <sup>11</sup>	0.5-5x10 <sup>12</sup>
N-6H/wet	negligible	0-2x10 <sup>11</sup>
p-6H/wet	mid 10 <sup>12</sup>	0.15-5x10 <sup>12</sup>

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These seemingly inconsistent results probably reflect the variety of measurement techniques used. As Table 1 demonstrates, the largest variations are in the reported interface state densities. The net oxide charge is straightforward to measure with a standard capacitance-voltage (CV) sweep at room temperature. Accurately calculating the interface state density, however, can be quite challenging. Raynoud et al. (Christophe Raynoud, Jean-Lun Autran, Bernard Balland, Gerard Guillot, Claude Jaussaud and Thierry Billon, *J. Appl. Phys.* 76 (2) p. 993 (1994)); Shenoy, supra; and Ouisse, supra; have discussed the various methods that can be used and the assumptions and limitations that must be taken into account when determining interface state densities. Of all the different techniques, the conductance and high-low techniques seem to be the most consistent and repeatable.

Although the reported quantities of oxide defects vary significantly from group to group, the goals for high quality MOS applications are fairly well defined: Oxide charge less than  $1 \times 10^{11} \text{ cm}^{-2}$  and interface states less than  $5 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$ . As Table 1 demonstrates, the quality of thermal oxides on SiC needs dramatic improvement. There are, however, few reported techniques for improving oxide quality. To date, the largest improvements result from varying the insert/withdrawal conditions of the oxidation and the oxidation pre-clean. Shenoy et al. (J.N. Shenoy, G.L. Chindalore, M.R. Melloch, J.A. Cooper, Jr., J.W. Palmour, and K.G. Irvine *Inst. Phys. Conf. Ser. No* 141: Chapter 4, p. 449 (1994)) also report a minimum net oxide charge density of  $9 \times 10^{11} \text{ cm}^{-2}$ , and a interface state density of  $1.5 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ , which are 3-4 times lower than their earlier oxidation conditions.

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### Object and Summary of the Invention

Therefore, it is an object of the present invention to further improve the quality of SiC oxides. The invention meets this object with a method  
5 for obtaining improved oxide layers and resulting improved performance from oxide based devices. The method comprises exposing an oxide layer (existing, deposited, nitrided, or thermally grown, and typically predominantly silicon dioxide) on a silicon carbide  
10 layer to an oxidizing source gas at a temperature below the temperature at which SiC would begin to oxidize at a significant rate, while high enough to enable the oxidizing source gas to diffuse into the oxide layer, and while avoiding any substantial additional oxidation  
15 of the silicon carbide, and for a time sufficient to densify the oxide layer and improve the interface between the oxide layer and the silicon carbide layer.

The foregoing and other objects, advantages and features of the invention, and the manner in which  
20 the same are accomplished, will become more readily apparent upon consideration of the following detailed description of the invention taken in conjunction with the accompanying drawings, which illustrate preferred and exemplary embodiments, and wherein:

### Brief Description of the Drawings

Figure 1 is a plot of several equivalent parallel conductance ( $G_p/w$ ) versus frequency curves taken at 250°C at several biases on the best oxide grown at 1050°C. The calculated interface state  
30 densities varied from  $1.0-1.6 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ , on the 1.1V and 0.7 V curves respectively;

Figure 2 is a plot of net oxide change ( $Q_{\text{eff}}$ ) and interface state densities ( $D_{\text{IT}}$ ) versus oxidation temperature for several oxidations performed across the  
35 usable temperature range;



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Figure 3 is a comparison of net oxide charge densities on oxides grown at 1100°C, and then re-oxidized at 800°, 900°, and 950°C;

Figure 4 is a comparison of interface state densities on oxides grown at 1100°C, and then re-oxidized at 800°, 900° and 950°C;

Figure 5 is a comparison of net oxide charge densities on oxides grown at 1050°C, and then re-oxidized at 900°, 950° and 1000°C;

Figure 6 is a comparison of interface state densities on oxides grown at 1050°C, and then re-oxidized at 900°, 950° and 1000°C;

Figure 7 is a bar graph of dielectric breakdown strengths of deposited oxides after different re-oxidation conditions; and

Figure 8 is a plot of oxide charge and interface state densities versus reoxidation time and temperature.

#### Detailed Description

In a first embodiment the invention comprises a method of obtaining improved oxide layers and resulting improved performance from oxide based devices. The method comprises exposing an oxide layer (predominantly silicon dioxide) on a silicon carbide layer to an oxidizing source gas (also referred to as an "oxidizing atmosphere") at a temperature below the temperature at which silicon carbide would begin to oxidize at a significant rate, while high enough to enable the oxidizing source gas to diffuse into the oxide layer. Any substantial additional oxidation of the silicon carbide is avoided, and the exposure is carried out for a time sufficient to densify the oxide layer and improve the interface between the oxide layer and the silicon carbide layer.

In this regard, it is generally accepted that silicon carbide oxidizes only at negligible or very

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slow rates until the temperature reaches about 1000°C, after which thermal oxidization occurs on a more measurable basis. Even at 1050°C, however, oxidizing a 500Å layer can take as long as 20-30 hours.

5           Accordingly, the method can further include the step of producing the oxide layer prior to the exposure step, and if silicon carbide is thermally oxidized in accordance with the present invention, the oxidizing temperature is at least 1000°C and preferably  
10   between about 1050°C and 1300°C.

          It will be understood, however, that the method of exposing the oxide layer on the silicon carbide layer to an oxidizing source gas does not require that the oxide layer have been first produced  
15   by thermal oxidization. Alternatively, the oxide layer could be produced by other methods such as depositing an oxide layer on the silicon carbide layer for example using low pressure chemical vapor deposition (CVD) with silane gas ( $\text{SiH}_4$ ), and oxygen ( $\text{O}_2$ ), plasma deposited  
20   oxides, deposited oxynitrides, thermal oxynitrides, or any combination of deposited or thermal layers of oxides, nitrides, or oxynitrides.

          As used herein, the term "oxynitride" will refer to oxide layers that have been exposed to nitrous  
25   oxide ( $\text{N}_2\text{O}$ ) at high temperature to incorporate nitrogen, oxide layers grown in  $\text{N}_2\text{O}$  to incorporate nitrogen, and alternating layers (or other combinations) of silicon dioxide ( $\text{SiO}_2$ ) and silicon nitride ( $\text{Si}_3\text{N}_4$ ).

          As used herein, the term "silicon carbide  
30   layer" most preferably refers to either a single crystal silicon carbide substrate or a silicon carbide epitaxial layer. Silicon carbide has a number of polytypes, of which the 3C, 4H, 6H, and 15R polytypes are particularly useful in electronic devices, and the  
35   invention produces suitable results in these various polytypes.

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As noted above, because the oxidation rate of SiC is negligible below about 1000°C, the step of exposing the oxide to the oxidizing atmosphere is preferably carried out at between about 800°C and 1025°C. In general terms, the approximate upper limit of 1025°C prevents any substantial oxidation of the silicon carbide, while the approximate minimum temperature of 800°C enables the process to take place at reasonable rates, it being understood that all chemical reactions take place to some degree over a wide range of temperatures, but for practical purposes only proceed at macroscopically observable rates within more narrow temperature ranges.

In this regard, and as generally well understood by those familiar with silicon carbide, a crystal substrate or epilayer is usually presented for oxidation (or for deposition of oxides) along either its silicon face, its carbon face, or along one of the A-axes (e.g.  $[11\bar{2}0]$  or  $[1\bar{1}00]$ ) perpendicular to these faces. Because carbon oxidizes somewhat more easily than silicon (and thus faster if all other factors are substantially equal), the oxidation on the carbon face can be carried out at temperatures of between about 900 and 1300°C, and the reoxidation anneal can be carried out at temperatures of between about 600 and 1000°C. Similarly, the oxidation on the silicon face can be carried out at temperatures of between about 1000 and 1400°C, and the reoxidation anneal can be carried out at temperatures of between about 700 and 1100°C to obtain the same degree of oxidation at about the same rate.

The oxygen containing gas can be any oxygen containing gas that does not otherwise interfere with the chemical, physical or electronic characteristics of either the oxide or the silicon carbide layers. Appropriate gases can be selected from among oxygen, water vapor, oxygen in water vapor ("wet oxidation"),

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water vapor in a carrier gas, the various gas compounds formed from nitrogen and oxygen, and mixtures of any of these gases.

Accordingly, in a most preferred embodiment  
5 the method comprises thermally oxidizing a layer of silicon carbide at a temperature of about between 1050°C and 1100°C to produce the oxide layer on the layer of silicon carbide, and thereafter exposing the layers of oxide and silicon carbide to an oxidizing  
10 source gas at a temperature below about 1050°C and most preferably about 950°C, in the presence of water (i.e. "wet oxidation"), and while avoiding any substantial oxidation of the silicon carbide, and for a time sufficient to densify the oxidizing layer and improve  
15 the interface between the oxide layer and the silicon carbide layer.

In another embodiment, the invention comprises an improved silicon carbide and oxide structure. In this embodiment, the invention comprises  
20 a silicon carbide substrate and an oxide layer on the silicon carbide substrate, with the oxide layer having an interface state density less than  $1.6 \times 10^{11}$  per square centimeter per electron volt. In preferred embodiments, the interface state density is less than  
25  $1.5 \times 10^{11}$  per square centimeter per electron volt, and in the most preferred embodiments is less than  $1.1 \times 10^{11}$  per square centimeter per electron volt.

As in the method aspects of the invention, the silicon carbide can be either an epitaxial layer or  
30 a substrate, and can preferably be selected from the group consisting of 2H, 3C, 4H, 6H and 15R polytypes.

In yet another embodiment, the invention comprises a silicon carbide and oxide structure in which the oxide layer on the silicon carbide substrate  
35 has an oxide charge less than  $2.5 \times 10^{12} \text{ cm}^{-2}$ . In more preferred embodiments, the oxide charge is less than

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$1.5 \times 10^{12} \text{cm}^{-2}$  and in most preferred embodiments is less than  $1.1 \times 10^{12} \text{cm}^{-2}$ .

As in the other embodiments, the silicon carbide comprises a single crystal with the polytype selected from the group consisting of 2H, 3C, 4H, 6H and 15R and can be either an epitaxial layer or a substrate.

### Experimental Procedures

#### Sample preparation

10 Sample preparation began with p-type substrates doped with aluminum (Al) in the  $1-2 \times 10^{18} \text{cm}^{-3}$  range with 3  $\mu\text{m}$  epitaxial layers doped between  $2 \times 10^{15}$  and  $3 \times 10^{16} \text{cm}^{-3}$ . The samples were cleaned with a typical RCA/Huang clean and then oxidized. Samples were either  
15 inserted at ambient temperature, and withdrawn at the oxidation temperature in argon, or had oxides deposited. Thermal oxidations were carried out at temperatures ranging from  $1050^\circ\text{C}$  to  $1300^\circ\text{C}$  in a wet environment created by bubbling oxygen through de-  
20 ionized water at  $95^\circ\text{C}$ . The oxidation times were adjusted to maintain a target oxide thickness of  $500\text{\AA}$ , and varied from  $450-550\text{\AA}$ . Deposited oxides had oxide thicknesses of about  $350\text{\AA}$ . A one hour argon anneal followed oxidation at the oxidation temperature.  
25 Various post-oxidation annealing procedures in an oxidizing ambient were investigated on both thermal and deposited oxides by annealing at temperatures ranging from  $800^\circ\text{C}$  to  $1000^\circ\text{C}$  either in the same wet oxidation environment or in pure oxygen. This temperature range  
30 results in almost no further oxidation into the SiC substrate, but appears to complete the oxidation of any possible carbon compounds (B. Horneitz, H-J. Michel, J. Halbritter, *J. Mater. Res.*, 9 (12) p.3088 (1994)) and encourage proper oxide stoichiometry (1:2 Si:O).  
35 After oxidation and any of the various anneals, the metal layer was sputtered onto the oxide

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for the front-side contact. The back-side oxide was etched off using reactive ion etching (RIE). Some samples also received a back-side contact of 200 nm of Pt sputtered, but it was later determined that this was unnecessary. The front, or "gate" contact of the thermally oxidized samples was then patterned and etched with a commercial aluminum etchant, which was found to be quite efficient at etching molybdenum. Square capacitors were patterned in three different sizes, 200 $\mu$ m, 300 $\mu$ m and 400 $\mu$ m on a side with a large (>>100 times the area) contact nearby. The large front-side contact was used to make a contact to the substrate in parallel with the backside contact, which was found to minimize any effects from epitaxial layer non-uniformities or series resistance. Samples with deposited oxides were patterned by liftoff of molybdenum and gold (Mo/Au).

#### Oxide Quality Measurement

The net oxide charge was calculated from the flatband voltage ( $V_{fb}$ ), determined by a room temperature high frequency (500 kHz) capacitance-voltage (C-V) sweep. Flatband voltage is affected by a combination of charge trapped in the oxide, mobile ions in the oxide, charged border traps (D.M. Fleetwood, *IEEE Trans. Nucl. Sci.*, NS-39 (12) p.269 (1992)), and charged interface states. Separating the different components on SiC capacitors is very difficult because of the wide band gap, but all of these effects can be considered together as a "net" oxide charge. Improvement in the sum of these effects is a necessary first step to improve device operation.

Interface state density was determined using the standard conductance technique (Nicollian, supra) at high temperature. Measurements were taken using an MDC CSM/2 system with an HP4284A capacitance meter. The capacitance and conductance were measured at a

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constant voltage across a frequency range of 1 kHz to 1 MHz. This was repeated at a variety of biases, and the band bending for each bias determined from the parallel capacitance. Figure 1 shows the equivalent parallel  
5 conductance ( $G_f/w$ ) versus frequency curves from the best oxide (discussed below), and corresponds to a minimum interface state density of  $1.0 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ . The conductance technique was done at  $250^\circ\text{C}$  to measure a wider region of the band gap than can be measured at  
10 room temperature, and to reduce the band bending variation for better signal resolution. Higher temperatures (up to about  $350^\circ\text{C}$ ) are preferable for measurement purposes, but the molybdenum gate oxidizes too rapidly at temperatures above  $250^\circ\text{C}$ .

## 15 Results & Discussion

### Oxidation Temperature

A comparison of  $D_{it}$  and  $Q_{ox}$  for the oxides grown at temperatures between  $1050^\circ\text{C}$  and  $1300^\circ\text{C}$  is given in Figure 2. All oxidations in Figure 2 were  
20 produced in a wet environment and followed by a 1 hour argon anneal. Figure 2 shows an increase in both  $Q_{ox}$  and  $D_{it}$  as the oxide temperature is increased. It is also interesting to note that the interface state density plateaus at about  $1150^\circ\text{C}$ . Because the  
25 oxidation times become excessively long, oxidation temperatures below  $1050^\circ\text{C}$  are not very practical.

The oxide quality is dramatically improved by oxidizing at the lowest temperature possible. Although the oxidation time is quite lengthy at  $1050^\circ\text{C}$ , the  
30 improved oxide quality is well worth the invested time for most MOS device applications.

### Re-Oxidation Anneal on Thermal Oxides

As set forth above, the invention comprises a post-oxidation treatment that is also beneficial to the  
35 oxide quality. This treatment consists of an oxidation performed at a lower temperature after the bulk of the

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oxide has been grown. This anneal is also referred to herein as a "re-oxidation" anneal. The temperature range of the re-oxidation anneal is between about 800°C and 1000°C. This step oxidizes any impurities, e.g. residual carbon or dangling silicon bonds, but without oxidizing the SiC any further, and thus densifying the oxide, and improving the SiC/SiO<sub>2</sub> interface. Table 2 compares four samples with various post-oxidation treatments. The first row was not treated with a post-oxidation anneal. The second row was removed from the oxidation furnace using the "slow pull" procedure described by Shenoy, et al, supra. The last two rows had a wet or dry post-oxidation treatment at 900°C for 1.5 hours. (The argon anneal is done in-situ with oxidation and is not considered a post-oxidation treatment for ease of discussion herein. All thermal oxides received this anneal immediately following oxidation and prior to any reoxidation anneal.)

	<u>Post-Oxidation</u>	<u>Q<sub>ox</sub> (cm<sup>-2</sup>)</u>	<u>D<sub>it</sub> (cm<sup>-2</sup>/eV)</u>
20	None	4.0x10 <sup>12</sup>	7.1x10 <sup>11</sup>
	Slow Pull	2.3x10 <sup>12</sup>	3.2x10 <sup>11</sup>
	Wet	1.5x10 <sup>12</sup>	2.8x10 <sup>11</sup>
	Dry	3.9x10 <sup>12</sup>	1.5x10 <sup>12</sup>

TABLE 2

As demonstrated by the data in Table 2, the slow pull procedure improves oxide quality, which is in agreement with Shenoy's results. Even higher oxide quality, as evidenced by lowered net oxide charge and interface state densities, is obtained by following a standard oxidation with a wet re-oxidation procedure. The dry re-oxidation anneal doubles the interface state densities, when compared with the oxide that received no post-oxidation treatment.

Attempts at optimizing both the time and temperature of the wet re-oxidation process were made



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on both 1050°C and 1100°C thermal oxides. Figures 3 and 4 demonstrate the net oxide charge and interface state densities of samples oxidized at 1100°C that received various re-oxidation conditions. The temperature of the re-oxidation varied from 800°C to 950°C, and oxidation times of 1.5 and 3 hours were investigated. The horizontal line indicates the densities of identically oxidized samples, but which had no re-oxidation anneal.

For the oxides grown at 1100°C, the oxide charge density varies the most with the temperature of the re-oxidation anneal. The time of the re-oxidation anneal has almost no effect on the net oxide charge density, as seen by comparing the 1.5 and 3 hour data points at 900°C in Figure 4. Comparing the two 900°C points in Figure 4, however, it seems that the longer anneal times are slightly better than the shorter anneal times. The interface state density is strongly affected by the re-oxidation anneal temperature. For the 1100°C oxide, the longer times and 950°C temperature produce the best oxide, which results in lowering net oxide charge density by a factor of 2.5 and interface state densities by a factor of 4.

Figures 5 and 6 demonstrate the net oxide charge and interface state densities of samples oxidized at 1050°C. Re-oxidation anneal temperatures from 900°C to 1000°C and anneal times of 1.5, 3 and 5 hours were investigated. Again, the horizontal line indicates the quality level of samples oxidized under the same conditions, but which received no re-oxidation anneal.

For the oxides grown at 1050°C, the net oxide charge density changes dramatically with increased oxidation time, as seen by comparing the two data points at 900°C in Figure 5. Even with the longer, 5 hour time at 900°C, however, the 950°C re-oxidation anneal for 3 hours is still comparable. The interface

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state density, however, is not dramatically affected by the re-oxidation anneal time, as seen by comparing the two 900°C anneal times in Figure 6. The largest re-oxidation anneal variable for the oxides grown at

- 5 1050°C is the anneal temperature, which appears to be optimal at around 950°C. Net oxide charge is decreased by as much as a factor of 2, while interface states are decreased by as much as a factor of 2.5.

- For both the oxides grown at 1050°C and at  
10 1100°C, the optimal temperature for the re-oxidation anneal is 950°C. Increased anneal time also improves the oxide quality, but this is a secondary effect compared to the temperature. The optimal re-oxidation, at 950°C, dramatically reduces the net oxide charge and  
15 interface states, even for oxides grown at the optimal temperature, 1050°C.

#### Reoxidation Anneal on Deposited Oxides

- Poor dielectric strength has been associated with deposited oxides, which is usually blamed on their  
20 silicon rich stoichiometry. Silicon carbide has the distinct advantage of oxidizing only at extremely high temperatures, which would allow the deposited oxide to be "re-oxidized". This can be done by annealing the deposited oxide in an oxidizing environment at a  
25 temperature high enough to oxidize any silicon in the oxide, but low enough that no significant oxidation of SiC occurs. This step not only allows for good densification of the oxide, it also allows for the formation of a thermal SiO<sub>2</sub> interface without consuming  
30 any significant amount of SiC or introducing carbon into the oxide.

- The dielectric strengths of deposited oxides at room temperature and 350°C are illustrated in Figure 7. The highest dielectric strength of the samples re-oxidizing at 1000°C was a surprisingly high 12.4 MV/cm.  
35 This is higher than the intrinsic SiO<sub>2</sub> dielectric

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strength of 11.3 MV/cm, but the excess could be due to the metal/SiC work function difference or net oxide charge densities that are not considered in the calculated field.

5           As demonstrated in Figure 7, the 1000°C re-oxidation condition produces the highest dielectric strengths. Although the highest breakdown field is unaltered from room temperature to 350°C, the distribution is broader, as indicated by the striped  
10 cap which represents the range of the to 20% of the breakdown fields. The samples re-oxidized at 800° and 900°C have lower fields which are reduced even further at 350°C. The sample oxidized for 90 minutes at 900°C was better than the sample oxidized for only 45  
15 minutes. This behavior is consistent with excess silicon being present in deposited oxides, which can then be oxidized to achieve correct stoichiometry in the oxide layer.

          The interface state densities and net oxide  
20 charge densities of these samples are plotted for each of these samples in Figure 8. Again, better quality is achieved with more oxidation. Both the net oxide charge and the interface state densities decrease with increased time and temperature. Interface state  
25 densities are in the  $2-3 \times 10^{11} \text{cm}^{-2} \text{eV}^{-1}$  range, while net oxide charge is about  $1 \times 10^{12} \text{cm}^{-2}$  for the samples which received the 1000°C re-oxidation.

          In summary, the reoxidation anneal has been demonstrated to dramatically improve the quality of  
30 both the deposited and thermal oxides. The breakdown field problem with which deposited oxides have historically been plagued is effectively eliminated with a re-oxidation anneal. The net oxide charge is also greatly improved, and oxides can repeatedly be  
35 made with a net oxide charge density of  $1 \times 10^{12} \text{cm}^{-2}$ . Interface state densities of  $1 \times 10^{11} \text{cm}^{-2} \text{eV}^{-1}$  are now commonly produced using the invention. Compared with

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prior oxidation procedures (e.g. at 1150°C with no re-oxidation), net oxide charge has been lowered by a factor of 3, while interface states have been improved by an order of magnitude. These process improvements  
5 result in the largest reduction in the net oxide charge and interface state densities reported to date.

In the drawings and specification, there have been disclosed typical preferred embodiments of the invention and, although specific terms have been  
10 employed, they have been used in a generic and descriptive sense only and not for purposes of limitation, the scope of the invention being set forth in the following claims.

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## THAT WHICH IS CLAIMED IS:

1. A method of obtaining improved oxide layers and resulting improved performance from oxide based devices, the method comprising:

5 exposing an oxide layer on a silicon carbide layer to an oxidizing source gas at a temperature below the temperature at which SiC would begin to oxidize at a significant rate, while high enough to enable the oxidizing source gas to diffuse into the oxide layer, and while avoiding any substantial additional oxidation  
10 of the silicon carbide, and for a time sufficient to densify the oxide layer and improve the interface between the oxide layer and the silicon carbide layer.

2. A method according to Claim 1 and further comprising the step of producing the oxide layer on the  
15 silicon carbide layer prior to the step of exposing the oxide and silicon carbide to the oxidizing source gas, and by a method selected from the group consisting of: depositing an oxide layer on the silicon carbide layer, sputter depositing the oxide layer, plasma depositing  
20 the oxide layer, and producing an oxynitride layer.

3. A method according to Claim 1 further comprising the step of producing the oxide layer on the silicon carbide layer and thereafter thermally oxidizing the carbon face of the silicon carbide layer  
25 at temperatures of between about 900° and 1300°C; and the step of exposing the oxide layer to an oxidizing source gas comprises exposing the oxide layer at temperatures of between about 600° and 1000°C.

4. A method according to Claim 1 further  
30 comprising the step of producing the oxide layer on the silicon carbide layer and thereafter thermally oxidizing the silicon face of the silicon carbide layer at temperatures of between about 1000° and 1400°C; and

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the step of exposing the oxide layer to an oxidizing source gas comprises exposing the oxide layer at temperatures of between about 700° and 1100°C.

5        5. A method according to Claim 1 wherein the  
step of exposing the oxide and silicon carbide to the  
oxidizing source gas comprises exposing an oxide layer  
on a silicon carbide epitaxial layer or an oxide layer  
on a silicon carbide substrate.

10       6. A method according to Claim 1 wherein the  
step of exposing the oxide and silicon carbide to an  
oxidizing source gas comprises exposing the oxide and  
silicon carbide to an oxygen-containing gas that does  
not otherwise interfere with the chemical, physical, or  
15       electronic characteristics of either of the oxide or  
silicon carbide layers, and exposing the oxide and  
silicon carbide to the oxygen-containing gas at a  
temperature of between about 800° and 1000°C.

20       7. A method according to Claim 1 wherein the  
step of exposing the oxide and silicon carbide to an  
oxidizing source gas comprises exposing the oxide and  
silicon carbide to a gas selected from the group  
consisting of: oxygen, water vapor, oxygen in water  
vapor, water vapor a in carrier gas, compounds of  
nitrogen and oxygen, and mixtures thereof.

25       8. A method according to Claim 1 and  
comprising:

thermally oxidizing a layer of silicon  
carbide at a temperature of between about 1050° and  
1100°C to produce an oxide layer on the layer of  
30       silicon carbide; and wherein

the step of exposing the oxide layer  
comprises exposing the layers of oxide and silicon

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carbide to an oxidizing source gas at a temperature below 1050°C.

9. A method according to Claim 8 wherein the step of thermally oxidizing a silicon carbide layer  
5 comprises thermally oxidizing a silicon carbide epitaxial layer or a silicon carbide substrate.

10. A method according to Claim 8 wherein the step of exposing the oxide and silicon carbide to an oxidizing source gas comprises exposing the oxide  
10 and silicon carbide to an oxidizing source gas at a temperature of about 950°C.

11. A method according to Claim 1 or Claim 8 and further comprising the step of annealing the oxide layer in an argon atmosphere prior to the step of  
15 exposing the layers to an oxidizing source gas.

12. An improved silicon carbide and oxide structure comprising:  
a silicon carbide substrate; and  
an oxide layer on the silicon carbide  
20 substrate, said oxide layer having an interface state density less than  $1.6 \times 10^{11}$  per square centimeter per electron-volt ( $\text{cm}^{-2}/\text{eV}$ ).

13. A silicon carbide and oxide structure according to Claim 12 wherein said interface state  
25 density is less than  $1.5 \times 10^{11} \text{ cm}^{-2}/\text{eV}$ .

14. A silicon carbide and oxide structure according to Claim 12 wherein said interface state density is less than  $1.1 \times 10^{11} \text{ cm}^{-2}/\text{eV}$ .

15. An improved silicon carbide and oxide  
30 structure comprising:

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a silicon carbide substrate; and  
an oxide layer on the silicon carbide  
substrate, said oxide layer having an oxide charge less  
than  $2.5 \times 10^{12} \text{ cm}^{-2}$ .

5            16. A silicon carbide and oxide structure  
according to Claim 15 wherein said oxide charge is less  
than  $1.5 \times 10^{12} \text{ cm}^{-2}$ .

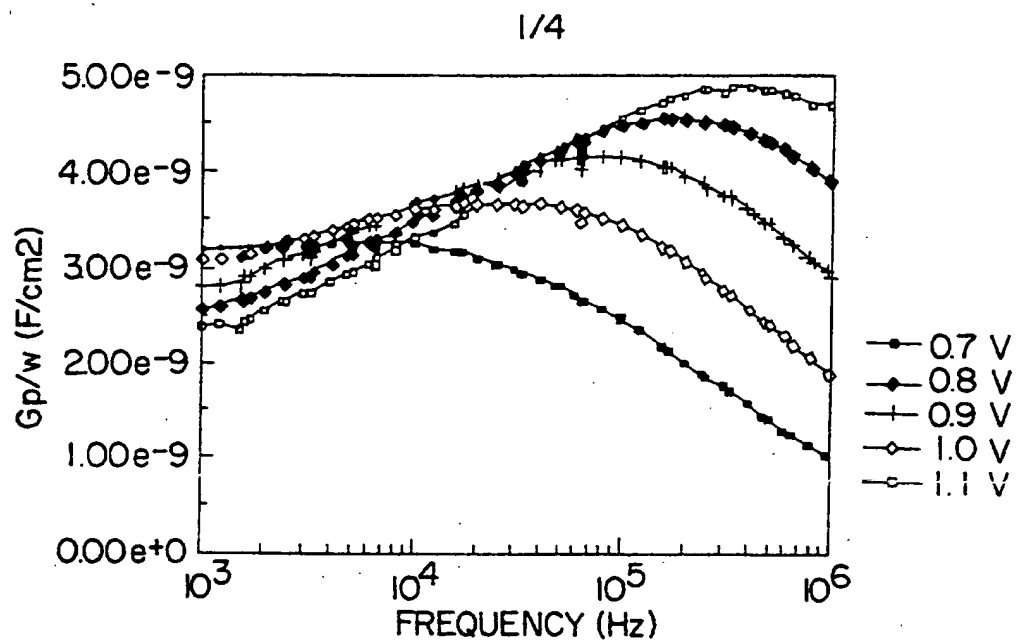
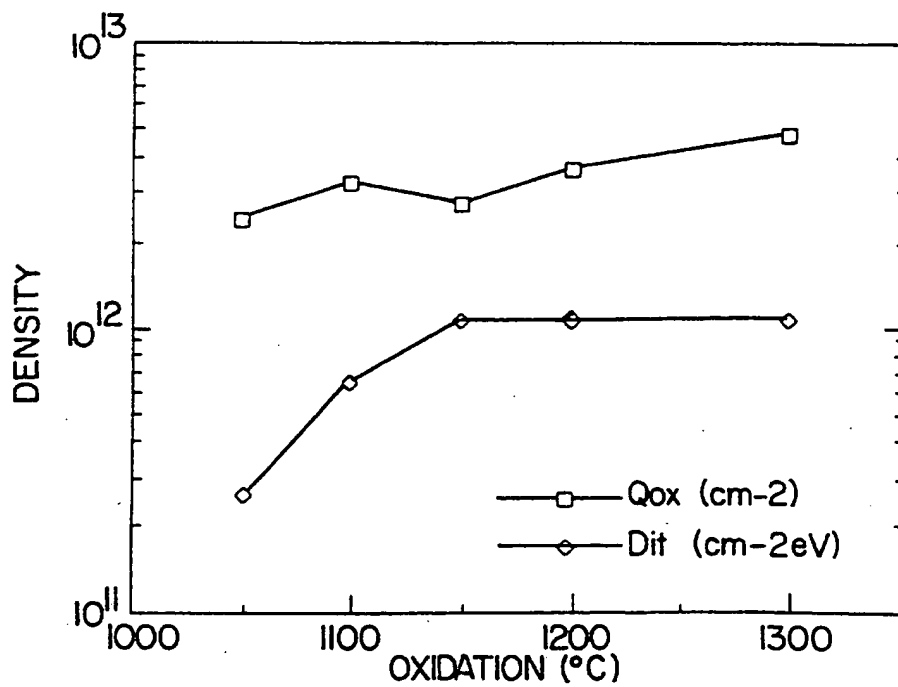
17. A silicon carbide and oxide structure  
according to Claim 15 wherein said oxide charge is less  
10 than  $1.1 \times 10^{12} \text{ cm}^{-2}$ .

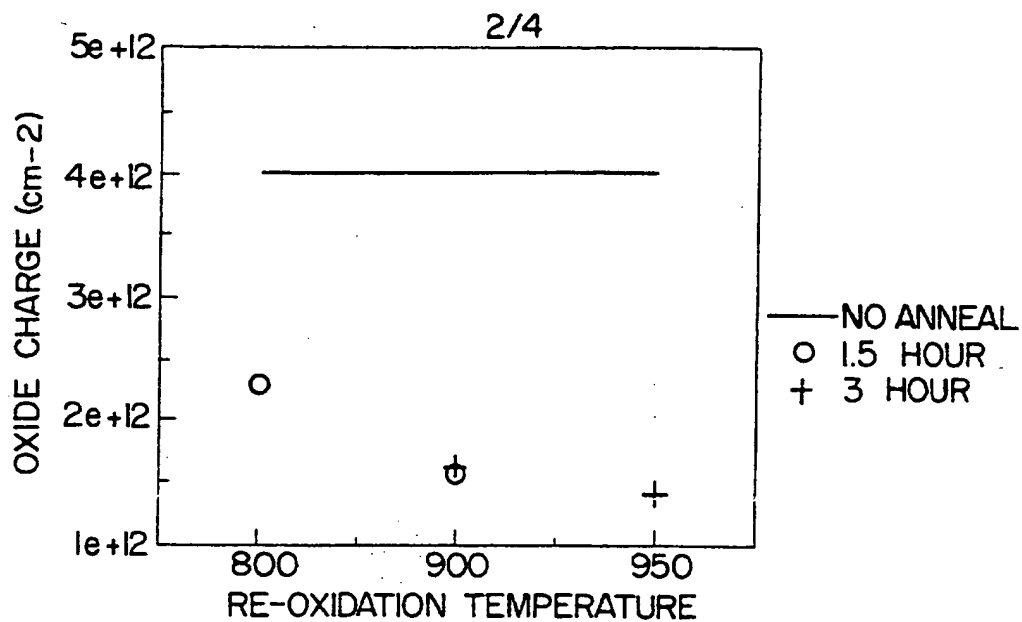
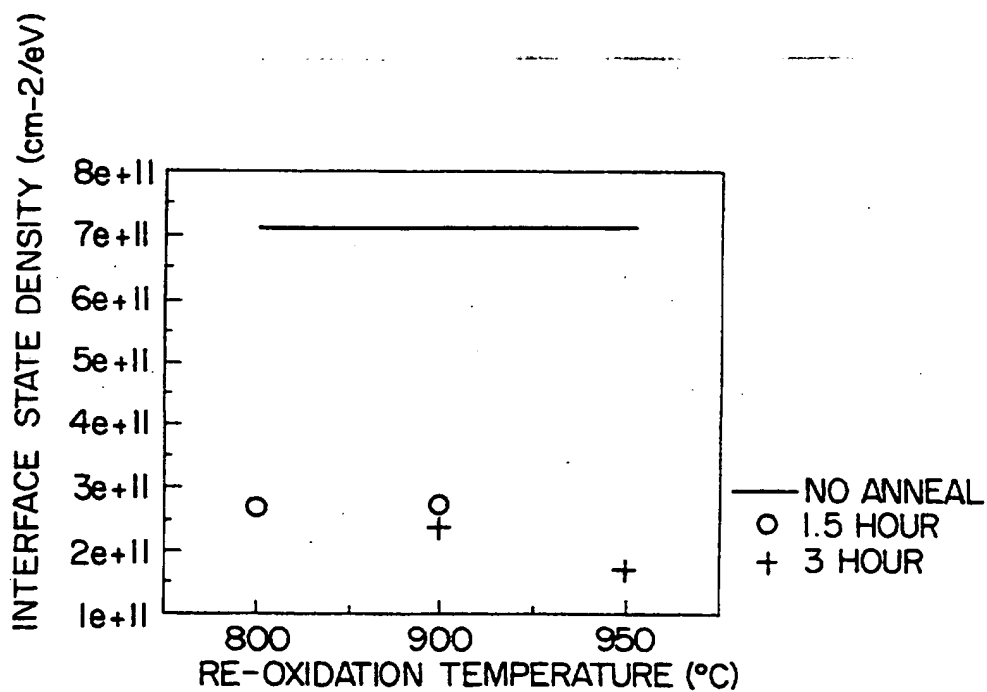
18. A silicon carbide and oxide structure  
according to Claim 12 or Claim 15 wherein said silicon  
carbide layer is a single crystal with a polytype  
selected from the group consisting of 2H, 3C, 4H, 6H,  
15 and 15R.

19. A silicon carbide and oxide structure  
according to Claim 12 or Claim 15 wherein said silicon  
carbide layer is an epitaxial layer or a substrate.

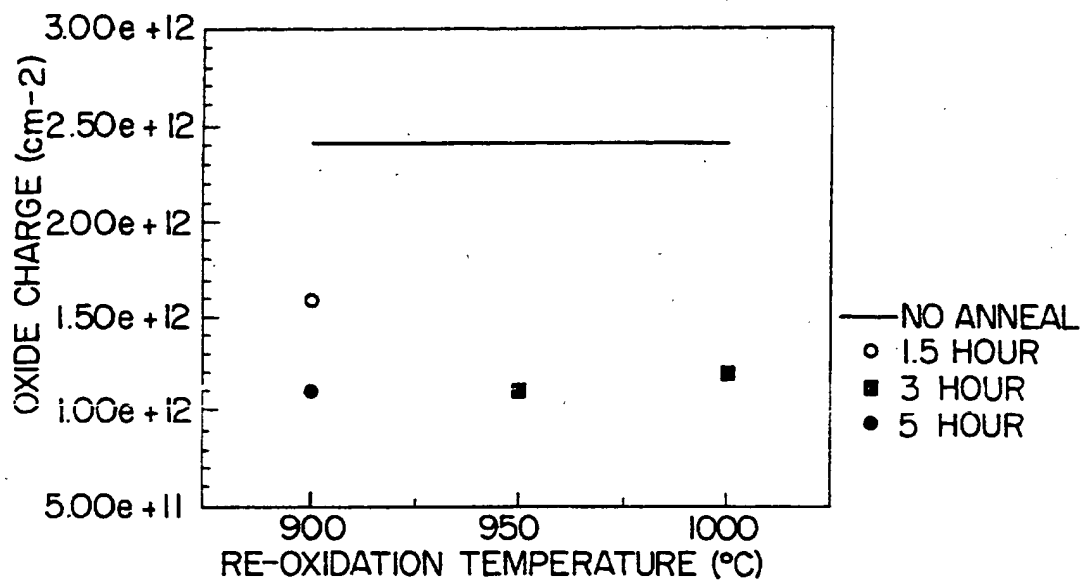
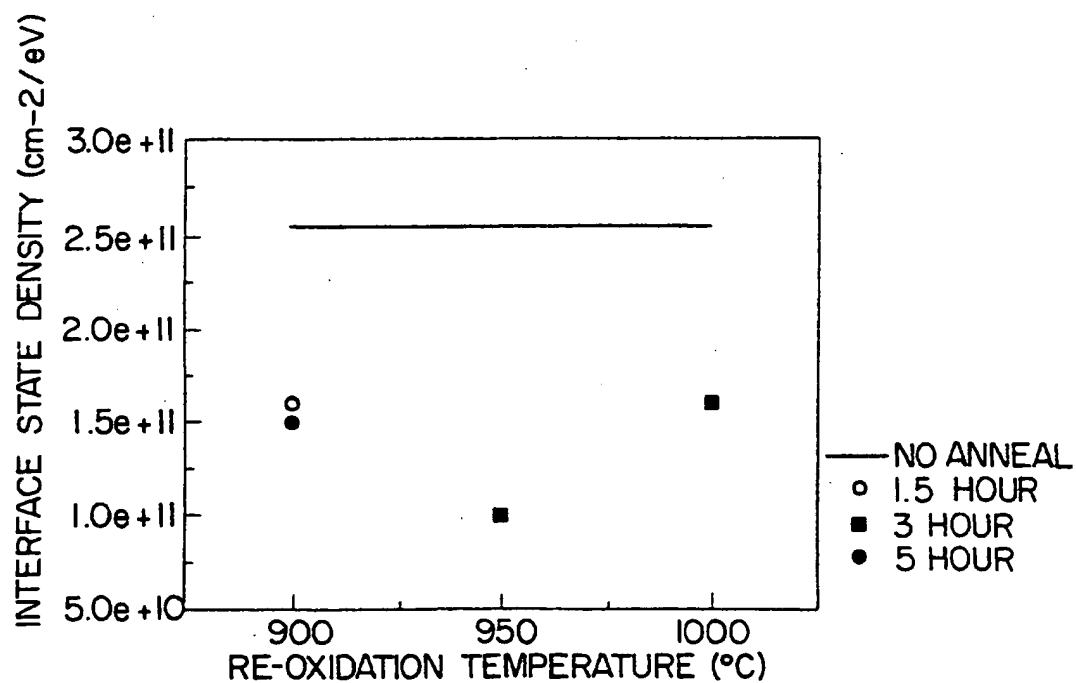
20. A silicon carbide and oxide structure  
20 according to Claim 12 or Claim 15 wherein said oxide  
layer is predominantly silicon dioxide.



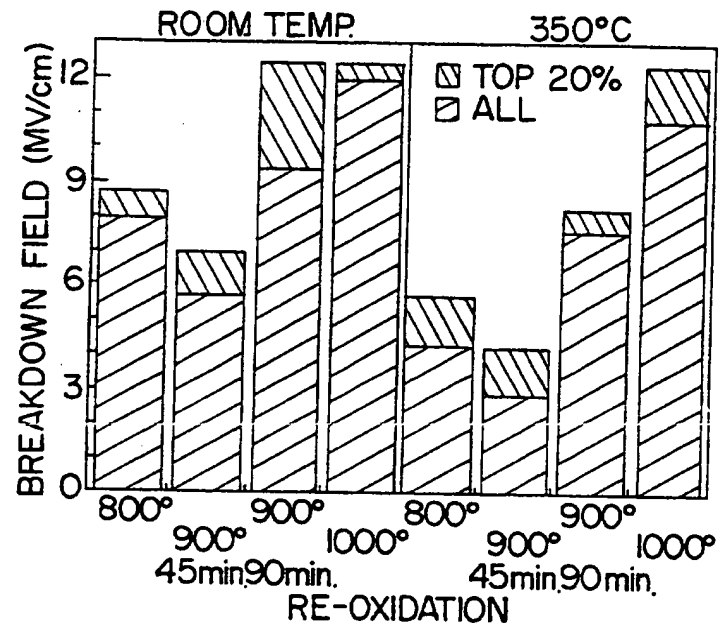
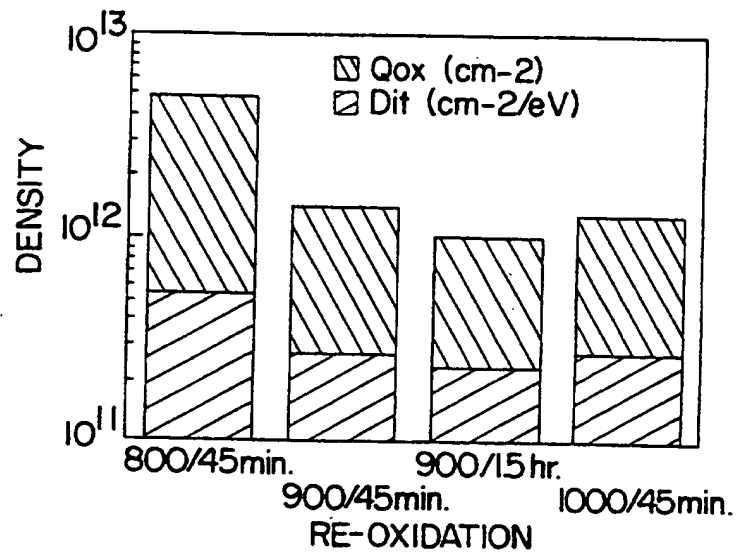
FIG. 1.FIG. 2.

FIG. 3.FIG. 4.

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FIG. 5.FIG. 6.

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FIG. 7.FIG. 8.

# INTERNATIONAL SEARCH REPORT

International Application No

PC1/US 96/17344

A. CLASSIFICATION OF SUBJECT MATTER  
IPC 6 H01L29/24 H01L21/02 H01L21/04

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JOURNAL OF THE ELECTROCHEMICAL SOCIETY, vol. 137, no. 1, 1 January 1990, pages 221-225, XP000133068 TANG S M ET AL: "HIGH FREQUENCY CAPACITANCE-VOLTAGE CHARACTERISTICS OF THERMALLY GROWN SiO2 FILMS ON B-SiC" see page 221, paragraph 4 see page 223, paragraph 3 - page 224, paragraph 2 ---	1-20
A	US,A,5 459 107 (PALMOUR JOHN W) 17 October 1995 see column 3, line 30 - column 4, line 20 see column 4, line 55 - column 5, line 10 see column 6, line 14 - column 6, line 25 --- -/--	1-10

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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Date of the actual completion of the international search

14 January 1997

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# INTERNATIONAL SEARCH REPORT

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## C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EXTENDED ABSTRACTS, vol. 89 / 2, 1 January 1989, pages 720-721, XP000277030 ZHENG Z ET AL: "FUNDAMENTAL OXIDATION STUDIES OF SINGLE CRYSTAL SiC" see page 720	1-10
A,P	US,A,5 506 421 (PALMOUR JOHN W) 9 April 1996 see column 4, line 56 - column 4, line 61 -----	1-10

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Information on patent family members

International Application No

PCT/US 96/17344

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US-A-5506421	09-04-96	AU-A- 5545894	22-06-94
		EP-A- 0671056	13-09-95
		JP-T- 8505492	11-06-96
		WO-A- 9413017	09-06-94